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(54) [Title of the Invention] ELECTROSTATIC BREAKDOWN PREVENTIVE CIRCUIT IN SEMICONDUCTOR DEVICE AND FORMING METHOD THEREOF

(57) [Summary]

[Purpose] To provide an electrostatic breakdown preventive circuit in a semiconductor device and a forming method thereof, in which while a sufficient resistance for voltage drop with respect to charge due to static electricity is maintained, wiring resistance in the circuit as a whole is reduced and size of a chip can be reduced.

[Structure] A source/drain portion 103 of an output transistor is formed over a single crystalline silicon semiconductor substrate. Then, a contact hole 106 which connects a

high-resistance wiring layer 104 and the source/drain portion 103 of the transistor is opened by a photolithography/etching technique. After that, the high-resistance wiring layer 104 is formed. Subsequently, a contact hole 105 is opened and an output pad 101 and an aluminum wiring 102 are formed. Components for obtaining resistance for voltage drop as an electrostatic breakdown preventive circuit are as follows and these three components are combined: sheet resistance of the high-resistance wiring layer 104, diameters of the contact holes 105 and 106, and the distance between the contact holes 103 and 104.

[Scope of Claims]

[Claim 1] An electrostatic breakdown preventive circuit in a semiconductor device, which protects an internal circuit from static electricity applied to an output terminal, comprising:

a high-resistance wiring layer which conducts voltage drop of charge due to static electricity and which is formed over a diffusion layer, which serves as a source/drain portion of an output transistor, with a first contact hole therebetween; and

a metal wiring which is connected to the output terminal and which is formed over the high-resistance wiring layer with a second contact hole therebetween.

[Claim 2] A forming method of an electrostatic breakdown preventive circuit in a semiconductor device, which protects an internal circuit from static electricity applied to an output terminal, comprising:

a step of forming a first contact hole which connects a source/drain portion of a transistor and a high-resistance wiring layer; and

a step of forming a second contact hole which connects the high-resistance wiring layer and a metal wiring which is connected to an output terminal,

wherein the first contact hole and the second contact hole are pattern formed so as to be adjacent to each other.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application] The present invention relates to an electrostatic breakdown preventive circuits, more specifically, to protective circuits which are provided on output terminal sides in semiconductor devices.

[0002]

[Related Art] FIGS. 2 show a structural example of an output protective circuit which has an electrostatic breakdown preventive function in a conventional semiconductor device, and (a) shows a plan view and (b) shows a cross-sectional view illustrated for easy understanding of the structure.

[0003] In the same drawings, a reference numeral 1 denotes an output pad which is formed of an aluminum alloy or the like, a reference numeral 2 denotes a contact hole which connects an output terminal and a high-resistance wiring 3 which is formed of polysilicon or the like, a reference numeral 4 denotes a contact hole which connects the high-resistance wiring layer 3 and an aluminum wiring 5 which leads to an output transistor, and a reference numeral 7 denotes a contact hole which connects the aluminum wiring 5 and a source/drain portion 6 which is formed in an n-type or p-type impurity diffusion layer of an input transistor.

[0004] In the circuit shown in FIGS. 2(a) and 2(b), in a case where charge due to static electricity is applied to the output pad portion 1, current flows due to source-drain breakdown in the output transistor, but the output transistor is protected by reduction in stress on the output transistor, because of voltage drop by the high-resistance wiring layer 3.

[0005]

[Problems to be Solved by the Invention] However, in the circuit shown in FIGS. 2(a) and 2(b), the high-resistance wiring layer 3 is connected in serial between the output pad 1 and the source/drain portion 6 of the output transistor. Accordingly, there is a problem in that wiring resistance of the high-resistance wiring layer 3 becomes large and circuit operation speed in the device as a whole becomes low. Further, there is also a problem in that an area occupied by the high-resistance wiring layer 3 is large, which prevents the size of a chip from being reduced.

[0006] An object of the present invention is to solve the foregoing problems such as increase in wiring resistance and prevention of reduction in size of a chip, and to provide an electrostatic breakdown preventive circuit in a semiconductor device and a forming method thereof, in which while a sufficient resistance for voltage drop with respect to charge due to static electricity is maintained, wiring resistance in the circuit as a whole is reduced and the size of a chip can be reduced.

[0007]

[Means and Operation for Solving the Problem] To solve the foregoing problems, in the present invention, an electrostatic breakdown preventive circuit in a semiconductor device, which protects

an internal circuit from static electricity applied to an output pad, includes a high-resistance wiring layer which conducts voltage drop of charge due to static electricity and which is formed over a diffusion layer which serves as a source/drain portion of an output transistor, with a first contact hole therebetween, and includes a metal wiring which is connected to the output pad and which is formed over the high-resistance wiring layer with a second contact hole therebetween.

[0008] In addition, according to the present invention, a forming method of an electrostatic breakdown preventive circuit in a semiconductor device, which protects an internal circuit from static electricity applied to an output pad, includes a step of forming a first contact hole which connects a source/drain portion of a transistor and a high-resistance wiring layer, and a step of forming a second contact hole which connects the high-resistance wiring layer and a metal wiring which is connected to an output pad, in which the first contact hole and the second contact hole are pattern formed so as to be adjacent to each other.

[0009]

[Embodiment] Next, an embodiment of an electrostatic breakdown preventive circuit in a semiconductor device and a forming method thereof of the present invention is described in detail with reference to the accompanying drawings.

[0010] FIGS. 1(a) and 1(b) are a plan view and a schematic cross-sectional view showing one embodiment of an electrostatic breakdown preventive circuit. Hereinafter, this embodiment is described with reference to these drawings.

[0011] First, an n-type impurity diffusion layer which serves as a source/drain portion 103 of an output transistor is formed over a single crystalline silicon semiconductor substrate by ion implantation of arsenic or the like. Then, a SiO_2 film is formed on a whole surface of the silicon substrate by an atmospheric pressure CVD method.

[0012] Next, a contact hole 106 which connects a high-resistance wiring layer 104 and the source/drain portion 103 of the transistor is opened by a photolithography/etching technique.

[0013] Subsequently, polysilicon is deposited, for example, by a reduced pressure CVD method. Resistance of this polysilicon film is adjusted by conducting ion implantation of arsenic or the like, and the high-resistance wiring layer 104 is formed by a photolithography/etching technique.

[0014] Then, a SiO_2 film is again deposited by an atmospheric pressure CVD method. Subsequently, a contact hole 105, which connects an aluminum wiring 102 which continues from

an output pad 101 and the aforementioned high-resistance wiring layer 104, is opened by a photolithography/etching technique. After that, aluminum is deposited by a sputtering method or the like and the output pad 101 and the aluminum wiring 102 are formed by a photolithography/etching technique.

[0015] Here, components for obtaining resistance for voltage drop which is equivalent to that of the conventional circuit are as follows and the resistance for voltage drop can be realized by appropriately combining these components: (1) sheet resistance of the high-resistance wiring layer 104, (2) diameters of the contact holes 105 and 106, and (3) the distance between the contact holes 103 and 104.

[0016] This is because resistance R of a wiring is defined as $R = \rho_s \cdot L \cdot W$. In this case, the foregoing (1), (2), and (3) correspond to ρ_s, W, and L, respectively. Note that a relationship between L and W is illustrated in FIGS. 1.

[0017] As the number of pairs of the contact holes 103 and 104 increases, the resistance R, determined by L, W, and ρ_s, which are connected in parallel between the output pad 101 and the source/drain portion 103 of the transistor, increases correspondingly, so wiring resistance in the circuit as a whole is reduced.

[0018] Further, as for reduction in size of a chip, since a high-resistance wiring layer is not provided between the output pad 101 and the aluminum wiring 102, layout of patterns can be reduced in size correspondingly, as can be appreciated by comparison between FIG. 1(a) and FIG. 2(a).

[0019]

[Effect of the Invention] Thus, according to the present invention, a high-resistance wiring layer which is necessary for voltage drop of charge due to static electricity is provided between an aluminum wiring and a diffusion layer, which serves as a source/drain portion of a transistor, and therefore, resistance between an output pad and the source/drain portion is reduced due to a serial arrangement of wiring resistance between contacts. In addition, since a high-resistance wiring layer between the output pad and the aluminum wiring becomes not necessary, it can be expected that operation speed of a circuit will become high and reduction in a chip area will be achieved.

[Brief Description of the Drawings]

[FIG. 1] A plan view and a cross-sectional view showing an embodiment of an electrostatic

breakdown preventive circuit in a semiconductor device of the present invention.

[FIG. 2] A conventional electrostatic breakdown preventive circuit in a semiconductor device.

[Reference Numerals]

101 input pad

102 aluminum wiring

103 source/drain portion of transistor

104 high-resistance wiring layer

105, 106 contact holes